ISSN: 2208-2735
Volume 03 Issue 04 2017
Available on-line at https://ijreee.com/index.php/eee/issue/view/123

DOI:https://doi.org/10.53555/eee.v3i4.378 *Received: 18-April-2017 Accepted: 22-May-2017*

FPGA BASED BL-CSC CONVERTER-FED BLDC MOTOR DRIVE WITH POWER FACTOR CORRECTION

Mr.K. Mohankumaramangalam PG Student,
Department of EEE,
Kathir College of Engineering, Coimbatore.
Mohanengr2010@gmail.com

Dr.B.Vaikundaselvan Professor & Head, Department of EEE,
Kathir College of Engineering, Coimbatore. vaikungth@yahoo.co.in

Mr.C.Sivan Raj
Assisant Professor, Department of EEE,
Kathir College of Engineering, Coimbatore.
reachsivanraj@gmail.com

Abstract — **This paper presents a Power Factor Correction (PFC) based Bridge Less Canonical Switching Cell (BL-CSC) converter-fed Brushless DC (BLDC) motor drive. The BL-CSC converter operating in a discontinuous inductor current mode is used to achieve a 0.99 power factor at the AC mains. The speed of the BLDC motor is controlled by varying the DC bus voltage using PI controller, where proportional and integral gains were tuned by conventional method. In order to reduce the switching losses of BLDC motor electronic commutation, Voltage Source Inverter (VSI) operates at fundamental frequency. Moreover, the bridgeless configuration of CSC converter offers low conduction losses due to partial elimination of diode bridge rectifier at the front end. The proposed configuration shows a considerable increase in efficiency.**

Keywords— ***BLDC Motor, VSI, CSC, BL-CSC, sensor-less, diode bridge rectifier.***

I. INTRODUCTION

Brushless DC (BLDC) motors are recommended for many low- and medium-power drives applications because of their high efficiency, high flux density per unit volume, low maintenance requirement, low Electromagnetic Interference (EMI) problems, high ruggedness , and a wide range of speed control. Due to these advantages, they find applications in numerous areas such as household application transportation (hybrid vehicle) aerospace heating, ventilation and air conditioning, motion control and robotics renewable energy applications etc.

The BLDC motor is a three-phase synchronous motor consisting of a stator having a three-phase concentrated windings and a rotor having permanent magnets. It does not have mechanical brushes and commutator assembly; hence, wear and tear of the brushes and sparking issues as in case of conventional DC machines are eliminated in BLDC motor and thus it has low EMI problems.

Conventional scheme of BLDC drive fed by an uncontrolled rectifier and a DC link capacitor followed by a three phase Pulse Width Modulation (PWM)-based VSI is used for feeding the BLDC. This type of scheme draws peaky, harmonic rich current from the supply and leads to a high value of Total Harmonic Distortion (THD) of supply current and very low power factor at AC mains. A very high

THD of supply current and very poor power factor of 0.72 is achieved which is not acceptable by IEC 61000-3-2.

These switching losses are reduced by using a concept of variable DC-link voltage for speed control of BLDC motor. This utilizes the VSI to operate in low frequency switching required for electronic communication of BLDC motor, hence reduces the switching losses associated with it The front end SEPIC AND CUK converter feeding BLDC motor using a variable voltage control have propos ed in and but at the cost of two current sensors.

This paper presents the development of a reduced sensor –based BLDC motor drive for low power application. This motor is also referred as an electronically commutated motor since an electronic commutation based on the Hall- effect rotor position signals is used rather than a mechanical commutation.

These types of PQ indices cannot comply with the international PQ standards such as IEC 61000-3-2. Hence, single-phase Power Factor Correction (PFC) converters are used to attain a unity PF at AC mains these converters have gained attention due to single-stage requirement for DC-link voltage control with unity PF at AC mains.

Selection of operating mode of the front-end converter is a tradeoff between the allowed stresses on PFC switch and cost of the overall system. Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) are the two different modes of operation in which a front-end converter is designed to operate. A voltage follower approach is one of the control techniques which are used for a PFC converter operating in the DCM.

This is BL-CSC converter designed to operate in Discontinuous Inductor Current Mode (DICM) Such that the current flowing through inductor l1 & l2 are discontinuous, whereas the voltage across the Intermediate capacitors C1& C2 remains continuous in a switching period. An approach of variable DC link voltage for controlling the speed of the BLDC motor is used and it electronically commutated for reduced switching losses in the VSI. DC Link voltage control done with PI control and

its optimized k_p and k_i constants estimated by using GENTIC ALGORITHEM.

II. BLOCK DIAGRAM

Fig. (1) Shows the system configuration of proposed BLDCM drive. As shown in the figure, an Uncontrolled Diode Bridge Rectifier (DBR) followed by a PFC-CSC converter is used for feeding the BLDCM via a three phase VSI. A sensor less control of BLDCM is used for the elimination of rotor position sensors for electronic commutation.

Where, ω_{c1} and ω_{c2} are the two corner frequencies where the constants a and T (time constant) are given as Equation (3.2),

$$a = \frac{1+\sin(\varphi_m)}{1-\sin(\varphi_m)} \; ; T = \frac{1}{\omega_m \sqrt{a}} \qquad (2)$$

Where, φ_m represents the required phase lead angle and ω_m represents the frequency corresponding to the maximum phase lead angle (φ_m).

Moreover, ω_m is also represented in Equation (3.3),

$$\log_{10}(\omega_m) = \frac{1}{2}\{\log_{10}(\omega_{c1}) + \log_{10}(\omega_{c2})\} \qquad (3)$$

The proposed drive is designed for achieving the control of speed over a wide range by varying the voltage at DC bus of VSI. Hence, the BLDCM is operated with fundamental switching frequency of VSI to achieve the electronic commutation for minimal switching losses in it.

When ac supply is given to Diode Bridge Rectifier (DBR), it converts AC signal to DC signal .The dc filter has the function to reduce the harmonic from the DBR. The Bridgeless Canonical Switching Cell (BL-CSC) is used to reduce the usage of diodes, no conduction loss occurs

.From BL-CSC converter, the voltage source inverter is fed into the BLDC motor, and the motor rotates .The PI controller and driver units are used to trigger the voltage source inverter. The FPGA controller has the voltage of minimum 5v, so driver unit is connected to the BL-CSC and

The value of constant 'a' is obtained from Equation (3.2) as 1.8944 and the time constant, T is calculated using Equation (3.3) as $1.44x10^{-3}$ rad/sec. Now to obtain a maximum phase shift of 18^0 at rated speed, corresponding to frequency of 80 Hz (i.e. $\omega_m \approx$ 503 rad/sec), Hence two corner frequencies, ωc1 and ωc2 are obtained as as $\omega_{c1} = 1/T = 692$ rad/sec and $\omega_{c2} = 1/(aT) = 365$ rad/sec.

Now substituting these values in Equation (3.1), one gets the transfer function of the required phase lead compensator as Equation (3.4),

$$G_c(s) = 1.8944\left(\frac{s+365}{s+692}\right) \quad (4)$$

VSI. Fig. (1) shows the block diagram of proposed method.

$$G_c(s) = \left(\frac{s+(1/R_aC_a)}{\quad / \quad / \quad}\right) \quad (5)$$

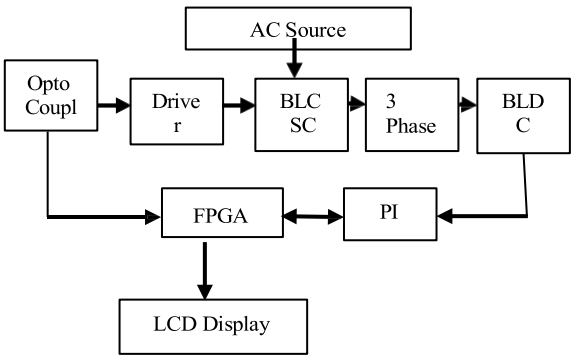

Figure 3.1 Block Diagram

III. DESIGN PROCEDURE

The phase lead compensator is designed to compensate a phase-delay (phase-lag) generated by sensing circuitry and a hysteresis comparator. The phase delay between the actual zero crossing of the line back-EMF and the virtual Hall signals are measured.

A phase-delay of 17-18^0 is obtained at the rated speed. Based on this evaluation, a phase-lead compensator is designed which transfer function is given as Eqn. (1),

$$s + (1\ R_aC_a + 1\ R_bC_a)$$

Hence by comparing this equation with Equation (3.4), the value of R_a and R_b are obtained as 27.4 kΩ and 30.6 kΩ (Ca = 0.1μF).

IV. RESULT AND DISCUSSION

A. Software Results

Input Voltage	50 V
Filter (LC)	L=$1.5e^{-3}$ and C= $330e^{-9}$
Switching Frequency	50 Hz
Motor	3 Phase BLDC
Set Speed	1200 rpm
Reference Speed	2000 rpm

$$G_c(s) = a\left(\frac{s+\omega_{c1}}{s+\omega_{c2}}\right) = a\left(\frac{s+1/aT}{s+1/T}\right) \quad (1)$$

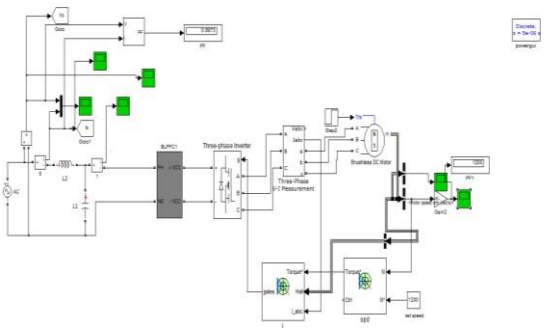

Fig. 2 MATLAB Simulation Diagram

Fig.2 shows the MATLAB simulation diagram of the FPGA based BL-CSC converter-fed BLDC motor drive. The input Voltage, current and Power of the circuit is as shown in the Fig. 3, 4 and 5.

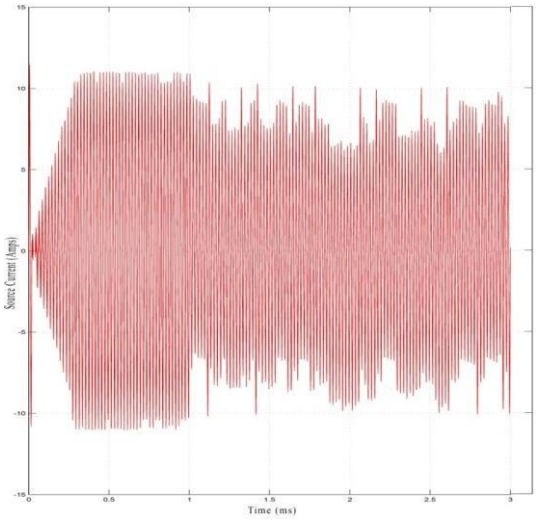

Fig. 3 Source Current

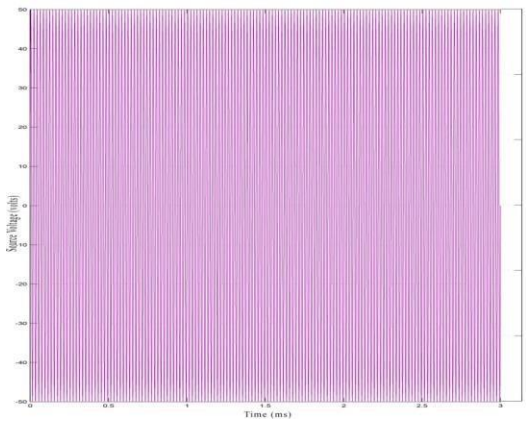

Fig. 4 Voltage

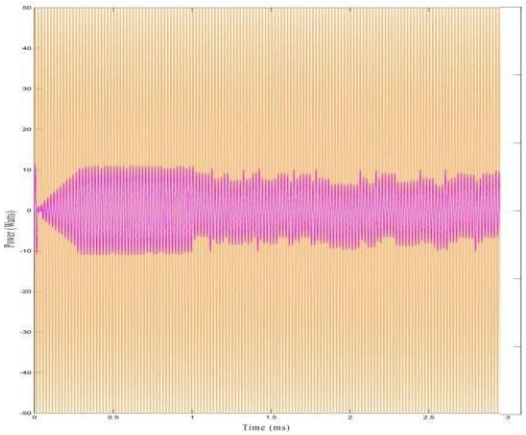

Fig. 5 Power

The filter current is as shown in the Fig. 6. Fig. 7 shows the motor torque and the speed of the rotor is as shown in the Fig. 8.

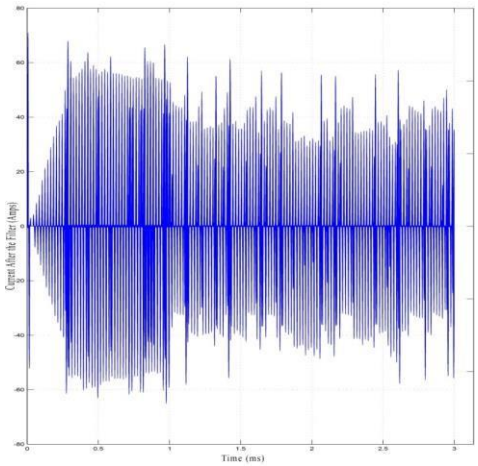

Fig. 6 Filter Current

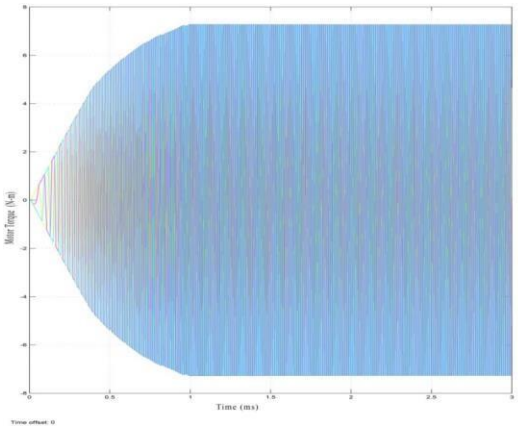

Fig. 7 Motor Torque

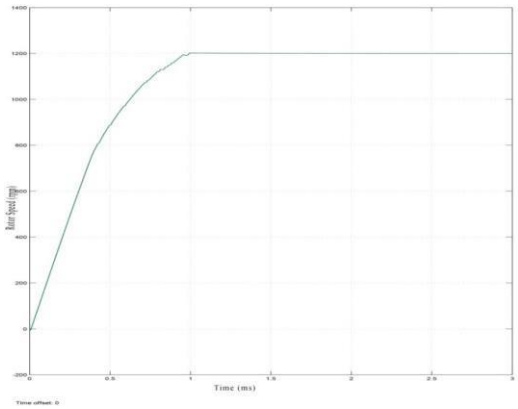

Fig. 8 Speed of the Rotor

B. Hardware Results

The hardware design for proposed FPGA based BL- CSC converter-fed BLDC motor drive is as shown in Figure 4.2. The hardware descriptions are,

- The experimental prototype with the proposed configuration is shown in Figure 4.2 and the design of the proposed system is shown in Figure 4.1.
- AHMY_SP6_LX9_LC is an easy to use FPGA Low cost board featuring Xilinx Spartan-6 FPGA. It is

specially designed for research, experimenting and learning system design with FPGAs.

- The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and an integrated photodetector. This unit is 8−lead DIP package.TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.
- The HCPL-4506 and HCPL-0466 contain a GaAsP LED while the HCPL-J456 and the HCNW4506 contain an AlGaAs LED. The hardware results are shown below, The BLDC stator current 1 and 2 are shown in Figure 5.1 and 5.2.

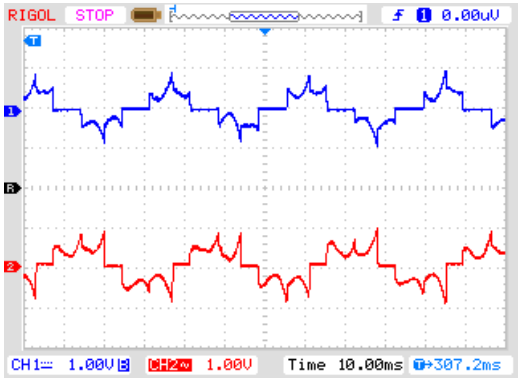

Fig. 9 BLDC Stator Current

The BLDC motor stator voltage and current is as shown in Fig. 9 and Fig. 10.

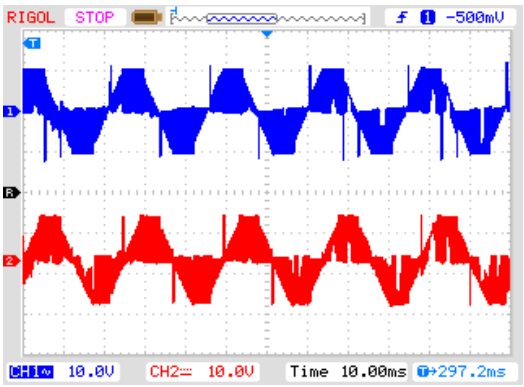

Fig. 10 BLDC Stator Voltage

The DC link voltage is as shown in Fig. 11 and the DC link voltage transient is as shown in Fig. 12

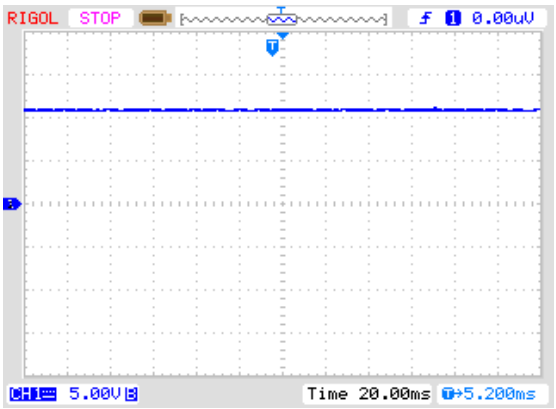

Fig. 11 DC Link Voltage

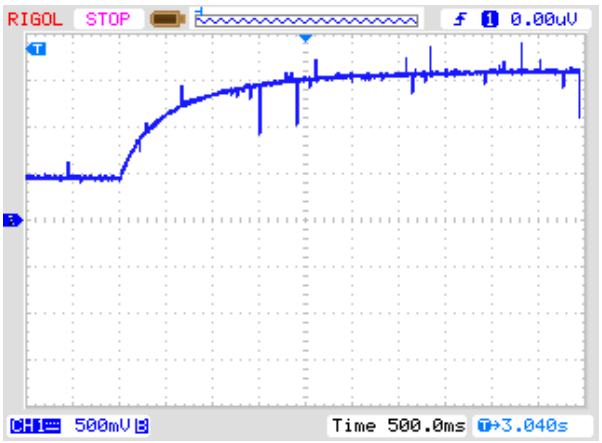

Fig. 12 DC Link Voltage Transient

The inductor current and source current before convertor ON state waveform is as shown in Fig. 13. The converter PWM signal is as shown in Fig. 14.

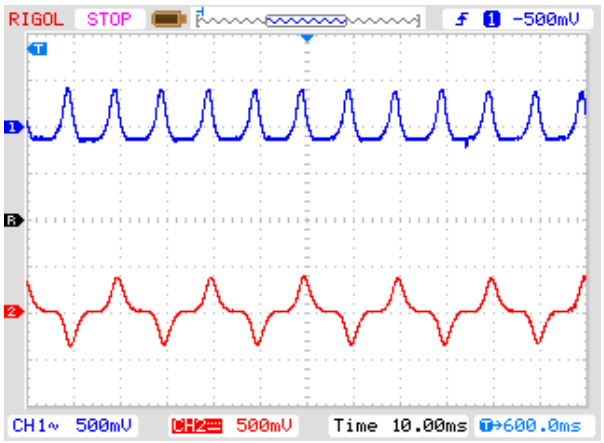

Fig. 13 Inductor Current and Source Current before Converter ON

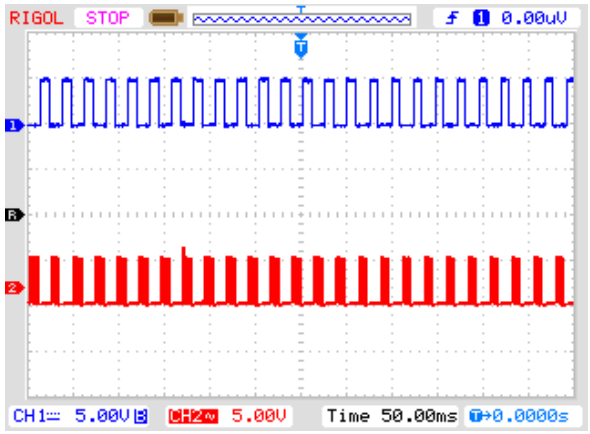

Fig. 14 PWM Waveform

Source current and FFT before converter switched ON state waveform is as shown in Fig. 15.

Source current and FFT after converter switched ON state waveform is as shown in Fig. 16.

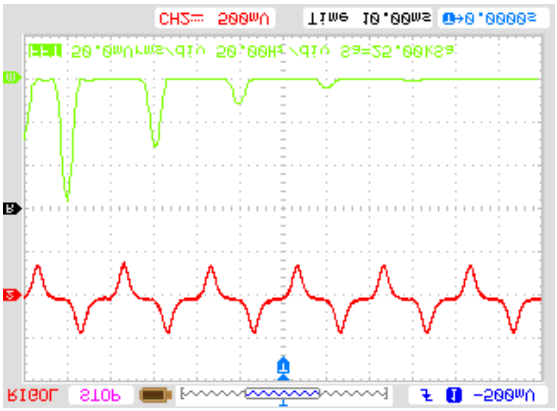

Fig. 15 Source Current and FFT before Converter Switched ON

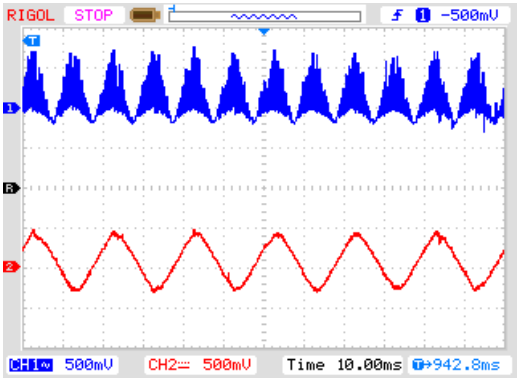

Fig. 16 Source Current and Inductor Current after Converter ON

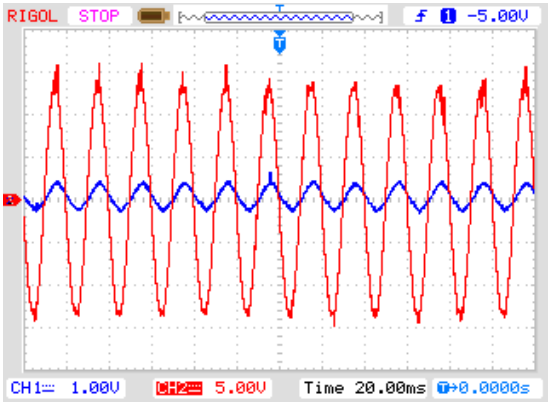

Fig. 17 Source Voltage and Current after Converter ON

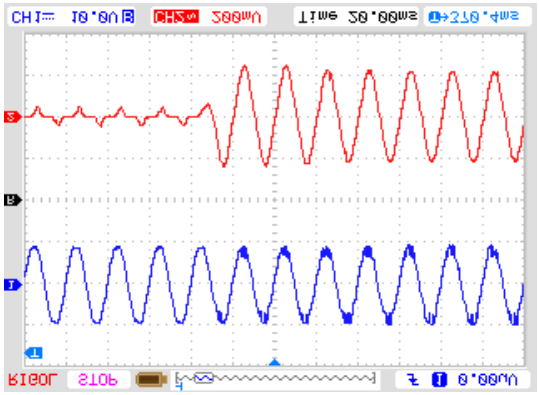

Fig. 18 Source Voltage and Current-Transient

Source voltage and current after converter ON state is as shown in Fig. 17. Source voltage and current transient is as shown in Fig. 18. The Source voltage and corresponding FFT is as shown in Fig. 19.

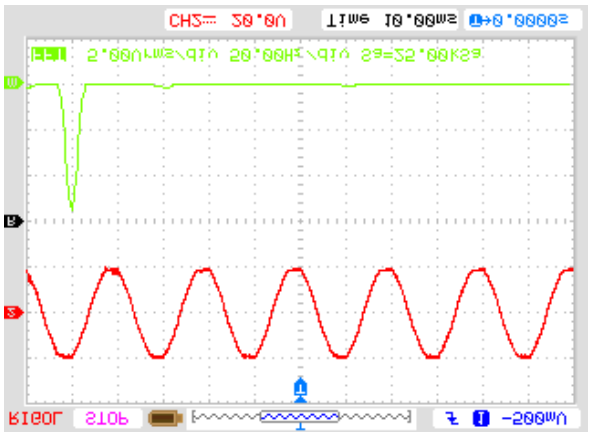

Fig. 19 Source Voltage and FFT

V. CONCLUSION

A sensor less BLDCM drive has been proposed as a cost effective solution for low power applications. The CSC converter has been designed for its operation in DICM for inherent power factor correction without any sensing requirements. The rotor position sensors have been eliminated by using the sensor less control of BLDCM to realize sensor less drive with power factor correction. The speed of the BLDCM has been controlled by varying the DC bus voltage of the VSI via a PFC-CSC converter. The BLDCM has been commutated electronically for the operation of VSI in low frequency switching for minimal switching losses in it. The proposed drive has shown a unity power factor operation at AC mains current harmonics.

REFERENCES

[1] Bist. V and Singh. B, (2014), 'An Adjustable Speed PFC Bridgeless Buck-Boost Converter Fed BLDC Motor Drive', IEEE Trans. Ind. Electron., Vol.61, No.6, pp.2665-2677.

[2] Bist. V and Singh. B, (2013), 'A Reduced Sensor PFC BL-Zeta Converter Based VSI Fed BLDC Motor Drive', Jr. Electric Power System Research, Vol.98, pp. 11–18.

[3] Bist. V and Singh. B, (2014), 'A PFC-Based BLDC Motor Drive Using a Canonical Switching Cell Converter,' IEEE Trans. Ind. Inform., Vol.10, No.2, pp.1207-1215.

[4] Chen. Y, Chiu. C, Jhang. Y, Tang. Z and Liang. R, (2013), 'A driver for the single phase brushless DC fan motor with hybrid winding structure,' IEEE Trans.Ind. Electron, Vol. 60, No. 10, pp. 4369–4375.

[5] Huang. X, Goodman. A, Gerada. C, Fang. Y and Lu. Q, (2012), 'A single sided matrix converter drive for a brushless DC motor in aerospace applications,' IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3542–3552.

[6] Kim. T.Y and Lyou. J, (2011), 'Commutation instant detector for sensorless drive of BLDC motor,' IEEE Electronics Letters, Vol.47, No.23, pp.1269-1270.

[7] Lai. Y.S and Lin.Y.K, (2008), 'Novel Back-EMF Detection Technique of Brushless DC Motor Drives for Wide Range Control without Using Current and Position Sensors,' IEEE Trans. Power Electron., Vol.23, No.2, pp.934-940.

[8] Mohan. N, Undeland. T. M and Robbins W. P, (2000), Power Electronics: Converters, Applications and Design. Hoboken, NJ, USA: Wiley, 2003. Limits for Harmonic Current Emissions (Equipment input current ≤16 A Per Phase), Int. Std. IEC 61000-3-2.

[9] Moreno. J, Ortuzar. M. E, and.Dixon. J. W, (2006), 'Energy-management system for a hybrid electric vehicle, using ultra capacitors and neural networks,' IEEE Trans. Ind. Electron., Vol. 53, No. 2, pp. 614– 623.

[10] Ozturk. S. B, O. Yang. O and Toliyat. H. A, (2007), 'Power factor correction of direct torque controlled brushless DC motor drive,' in Conf. Rec. 42nd IEEE IAS Annu. Meeting, 23–27, pp. 297–304.

[11] Pillay. P and Krishnan. R, (1988), 'Modeling of permanent magnet motor drives,' IEEE Trans. Ind. Electron., Vol. 35, No. 4, pp. 537–541.

[12] Rahman. M. A and P. Zhou. (1996), 'Analysis of brushless permanent magnet synchronous motors,' IEEE Trans. Ind. Electron., vol. 43, no. 2, pp. 256–267.

[13] Sago. O, Matsui. K, Mori. H, Yamamoto. I, Matsuo. M, Fujimatsu. I, Watanabe. Y and Ando. K, (2014), 'An optimum single phase PFC circuit using CSC converter,' Proc. of 30th IEEE-IECON, Vol.3, pp. 2684- 2689.

[14] Shao. J, Nolan. D, Teissier. M and Swanson. D, (2003), 'A novel microcontroller-based sensorless brushless DC (BLDC) motor drive for automotive fuel pumps,' IEEE Trans. Ind. Appl.,, Vol.39, No.6, pp.1734-1740.

[15] Singh. B and Singh. S, (2010), 'Single-phase power factor controller topologies for permanent magnet brushless DC motor drives,' IET Power Electron., Vol. 3, No. 2, pp. 147–175.

[16] Singh. B and Bist. V, (2013), "An Improved Power Quality Bridgeless Cuk Converter Fed BLDC Motor Drive for Air Conditioning System", IET Power Electron, Vol.6, No.5, pp. 902–913.

[17] Singh. B (2003) 'A review of single-phase improved power quality AC–DC converters,' IEEE Trans. Ind. Electron., Vol. 50, No. 5, pp. 962–981.

[18] Singh. B, Singh. S, Chandra. A and Al-Haddad. K, (2011), 'Comprehensive study of single-phase AC–DC power factor corrected converters with high-frequency isolation,' IEEE Trans. Ind. Informat., Vol. 7, No. 4, pp. 540–556.

[19] Su. G. J and McKeever. J.W, (2004), 'Low-cost sensorless control of brushless DC motors with improved speed range,' IEEE Trans. Power Electron., Vol.19, No.2, pp.296-302.

[20] Toliyat. H. A and Campbell. S, (2004), DSP-based Electromechanical Motion Control. New York, NY, USA: CRC Press.

[21] Xia. C. L, (2012), 'Permanent Magnet Brushless DC Motor Drives and Controls,' Hoboken, NJ, USA: Wiley.

[22] Wu. C.H and Tzou Y.Y, (2009), 'Digital control strategy for efficiency optimization of a BLDC motor driver with VOPFC,' in Proc. IEEE ECCE, 20–24, pp. 2528–2534.